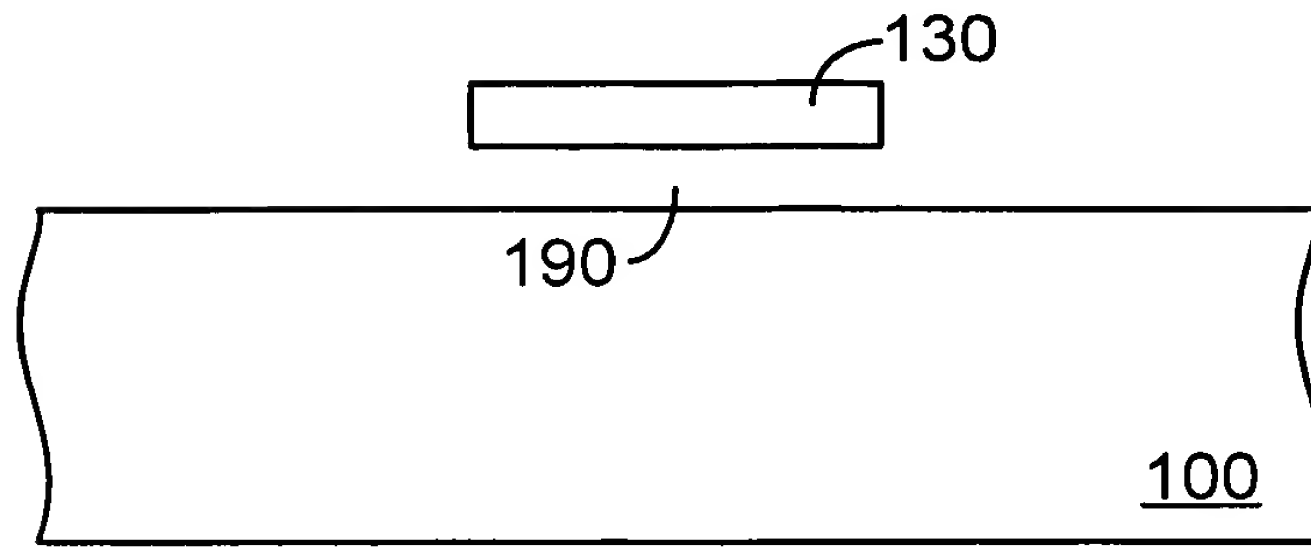


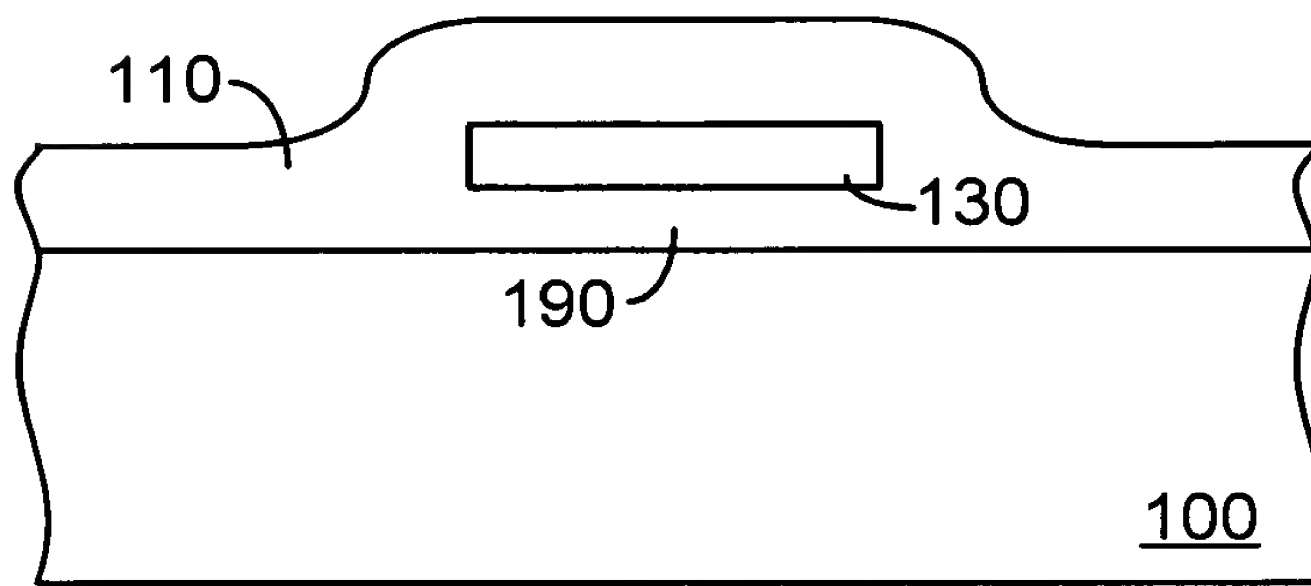


1/6

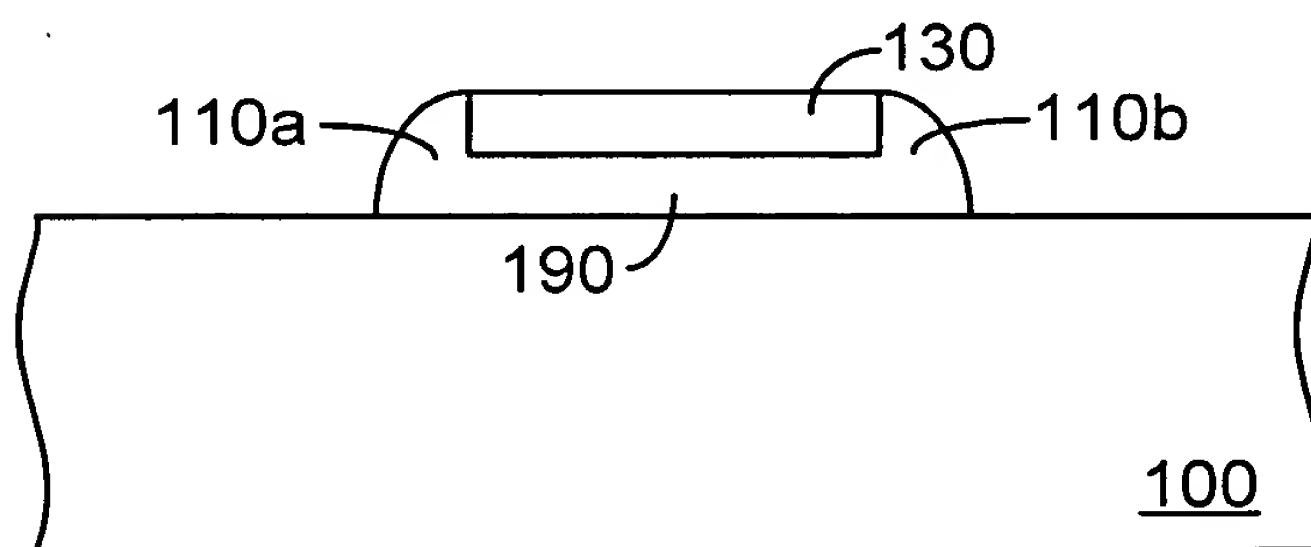
**Fig. 1a**



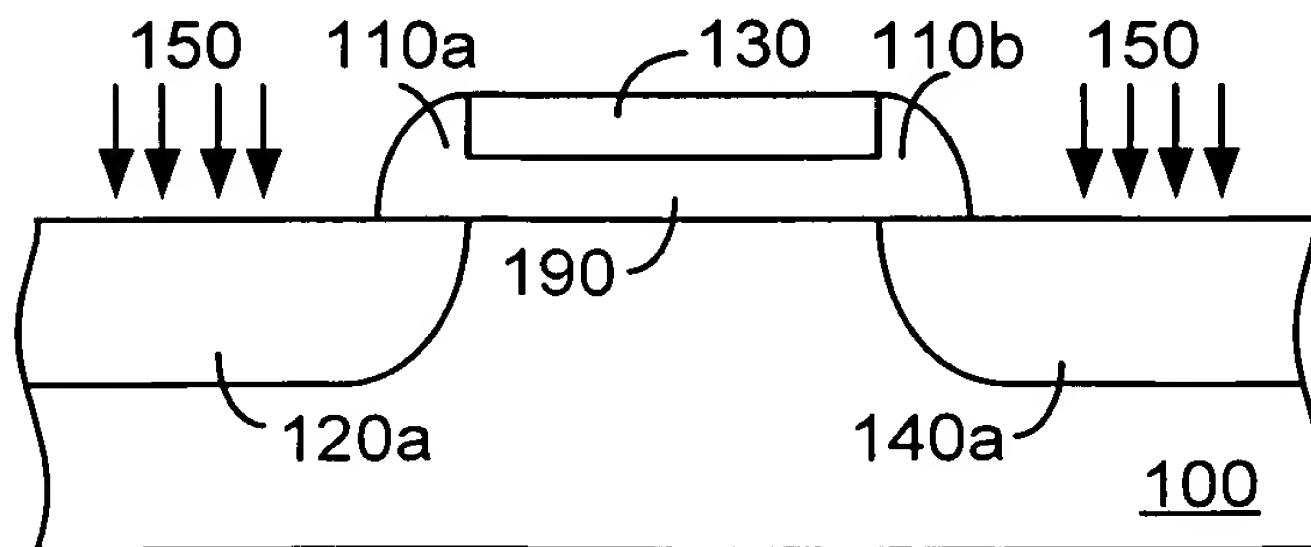
**Fig. 1b**

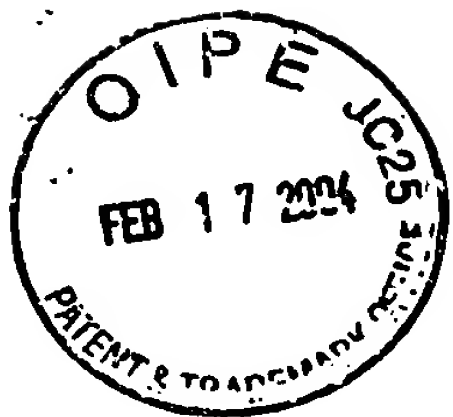


**Fig. 1c**



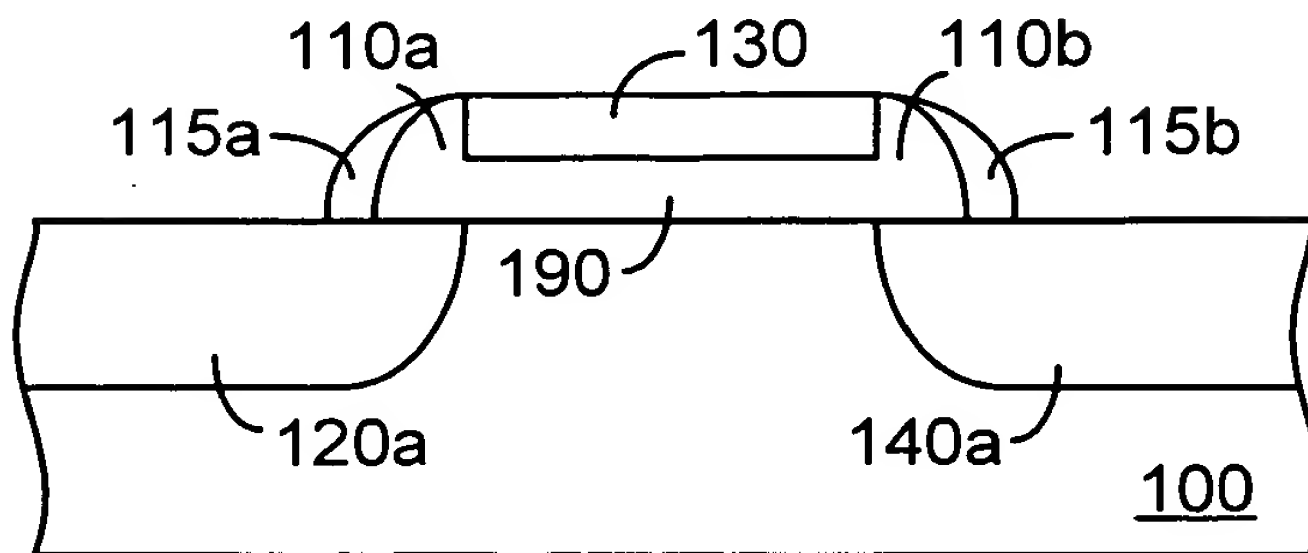
**Fig. 1d**



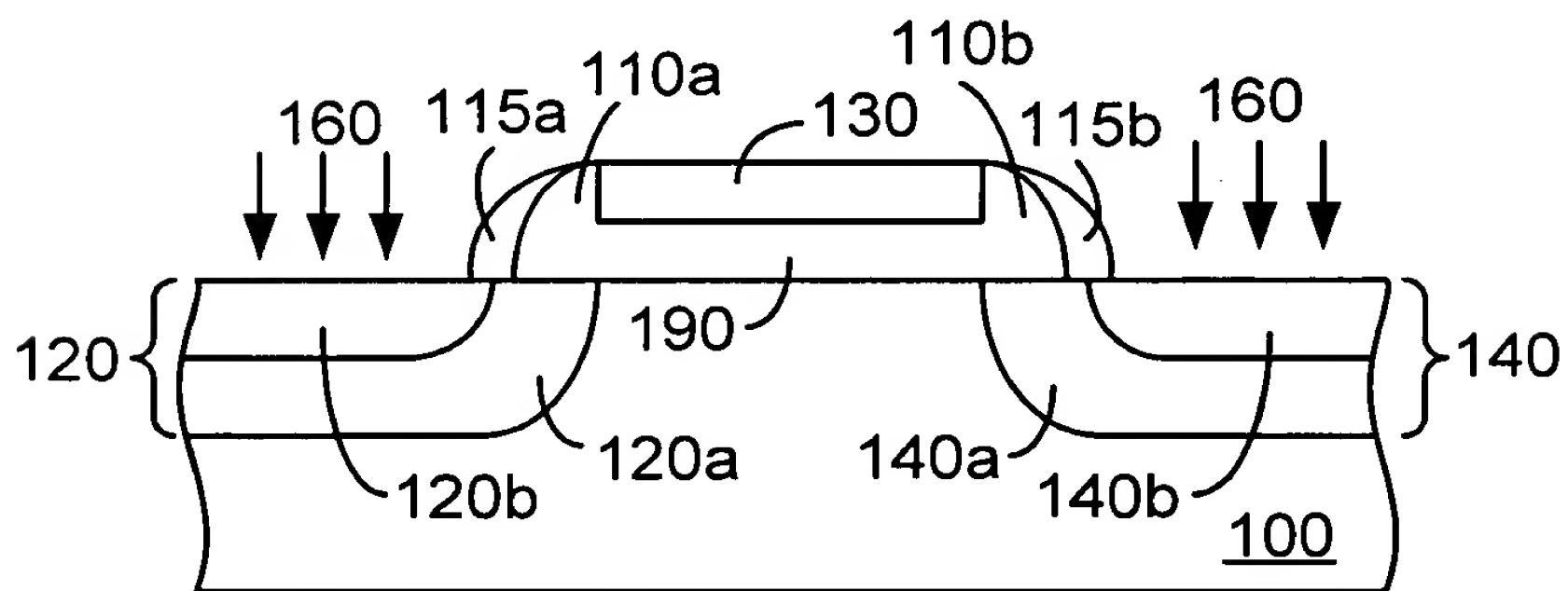


2/6

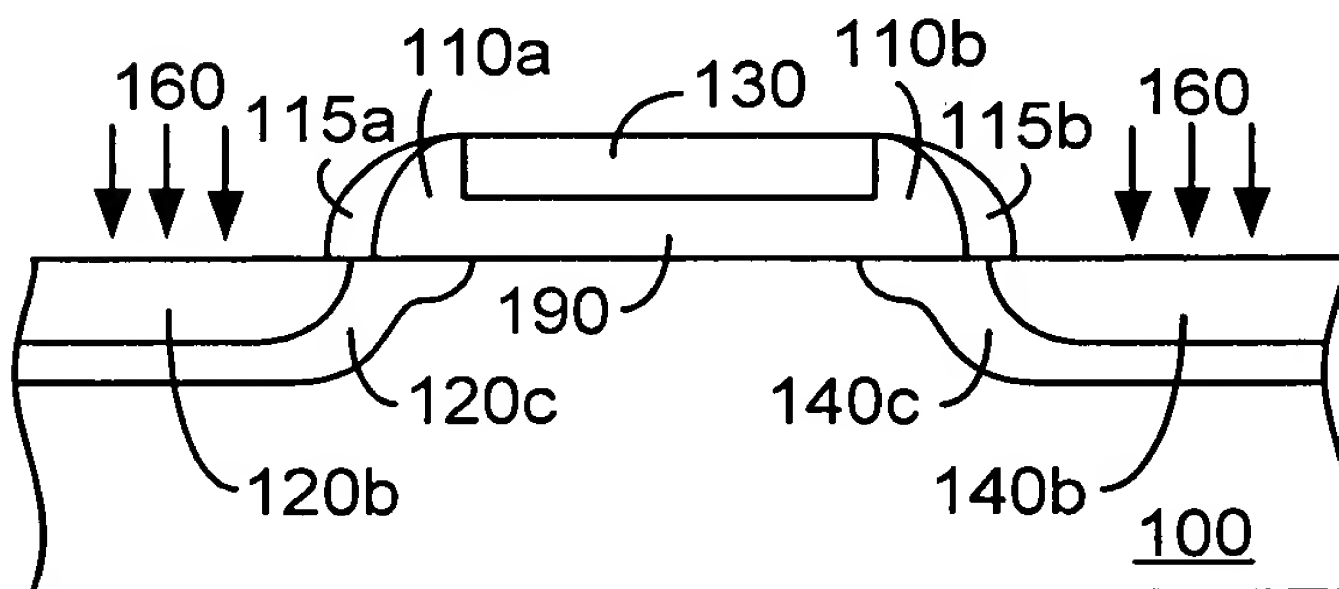
**Fig. 1e**

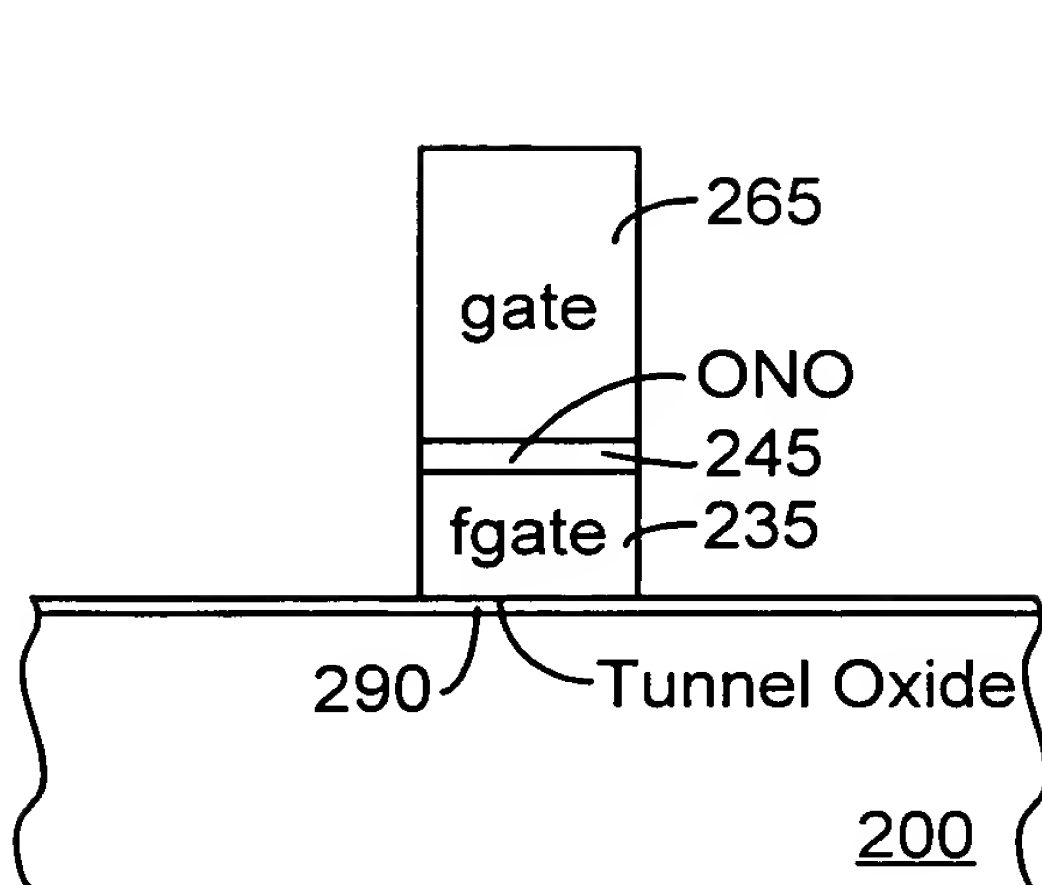
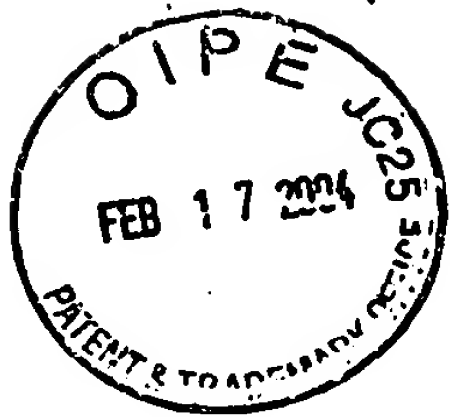


**Fig. 1f**

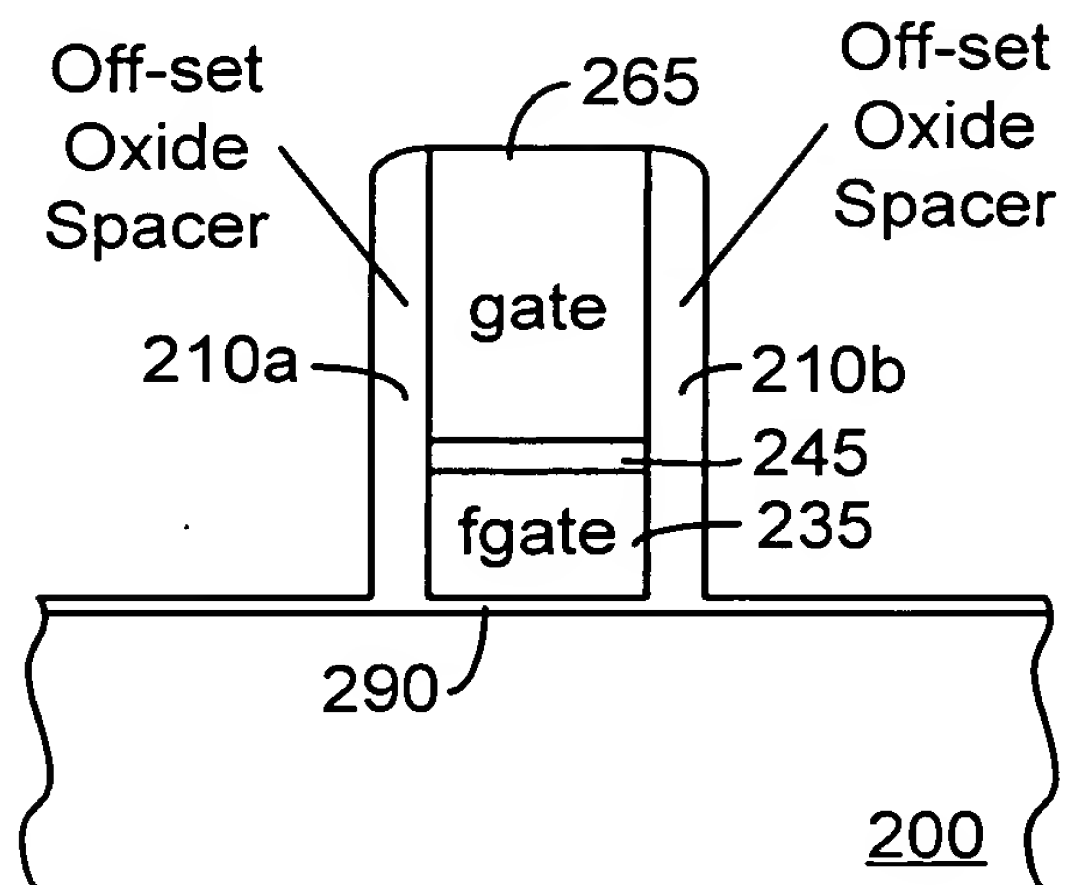


**Fig. 1g**

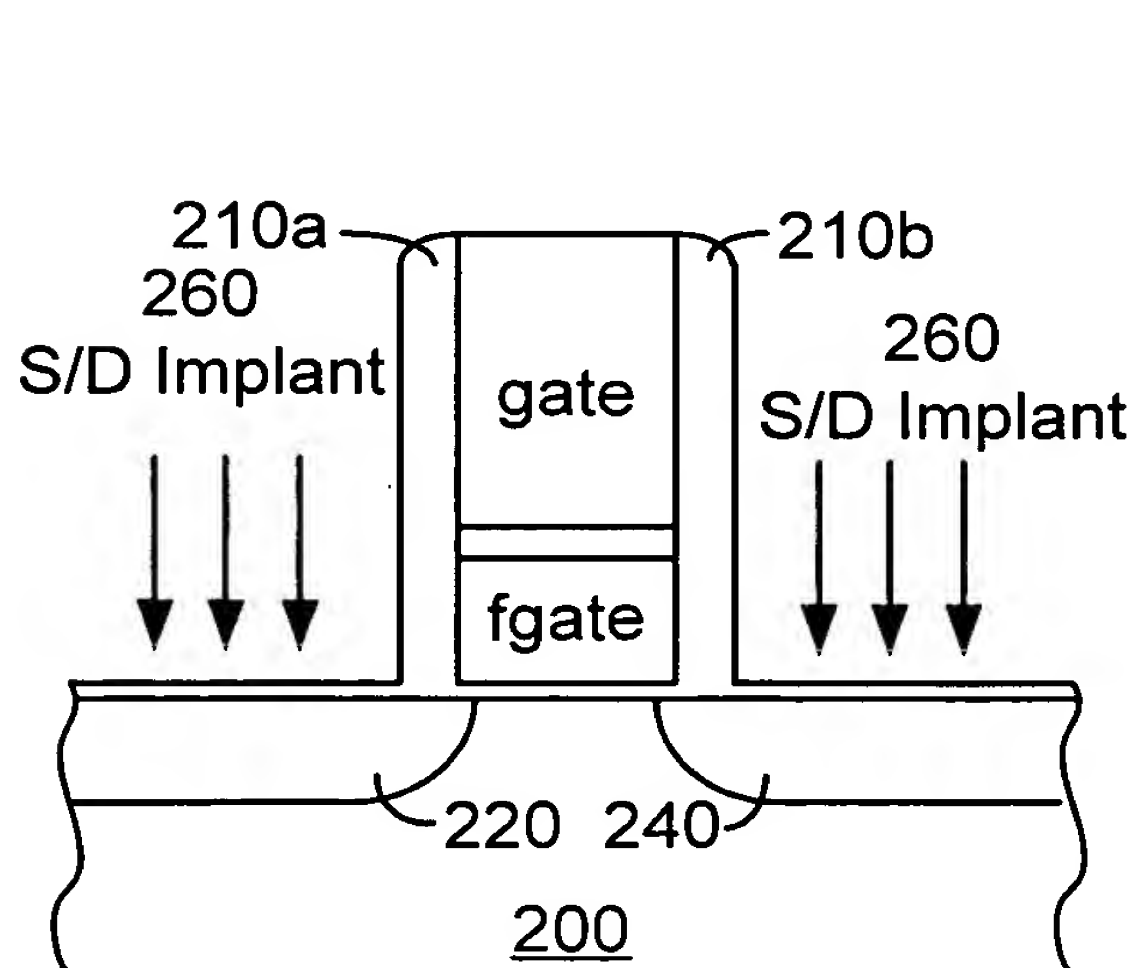




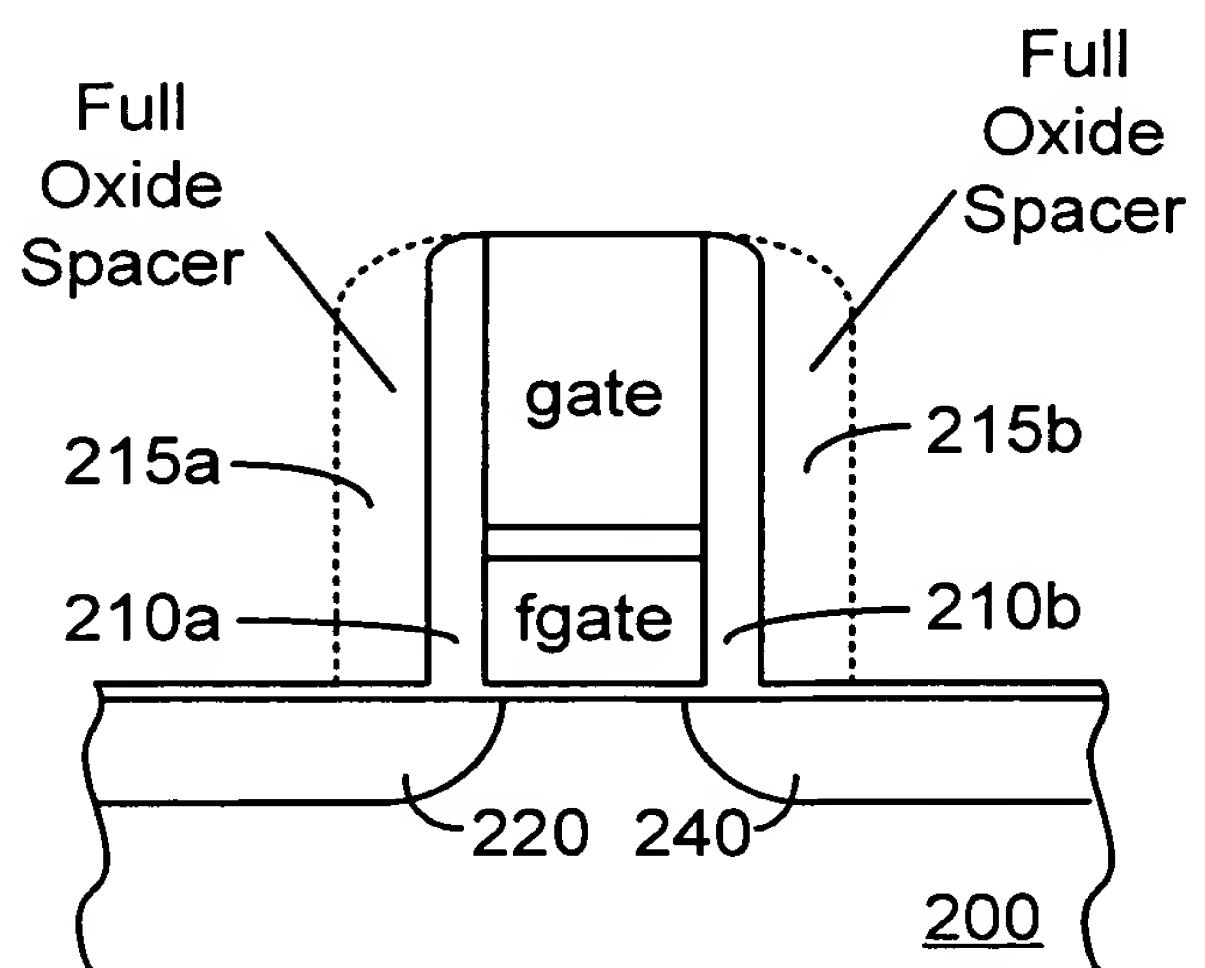
**Fig. 2a**



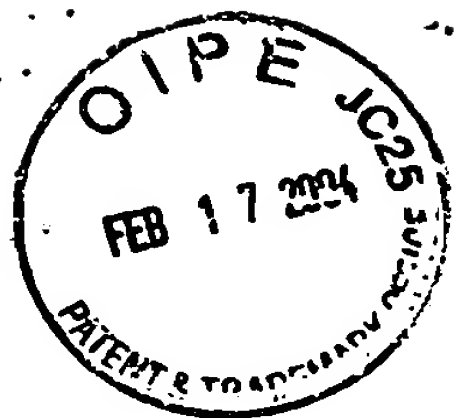
**Fig. 2b**



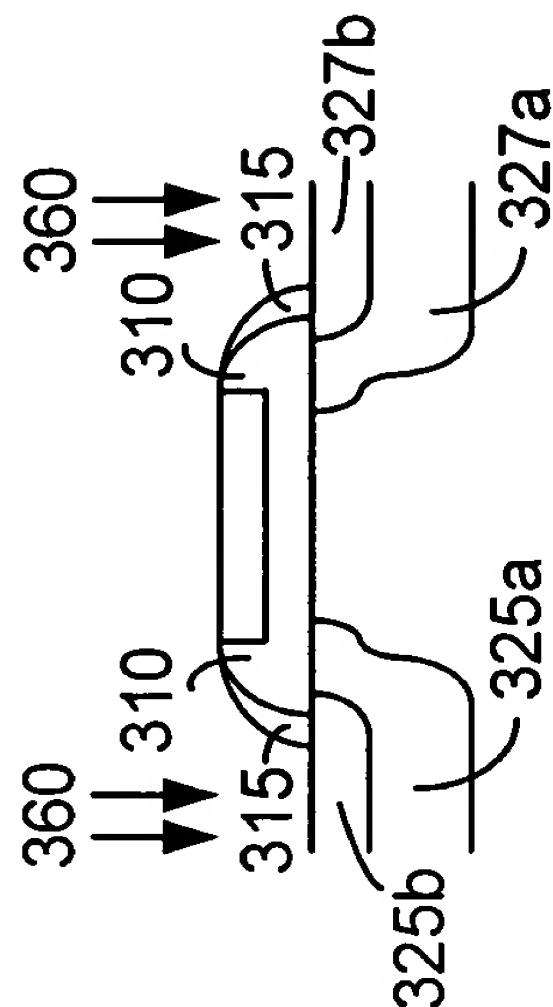
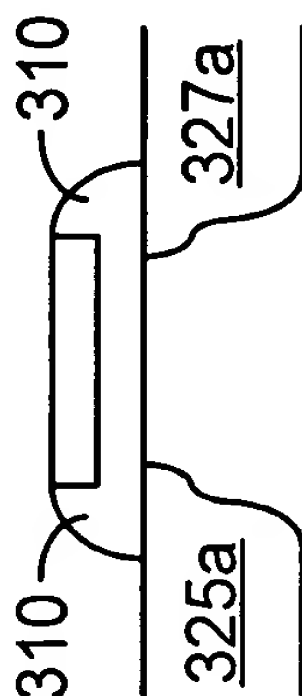
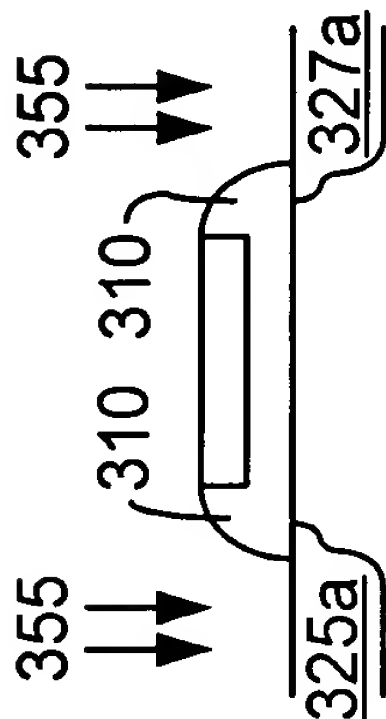
**Fig. 2c**



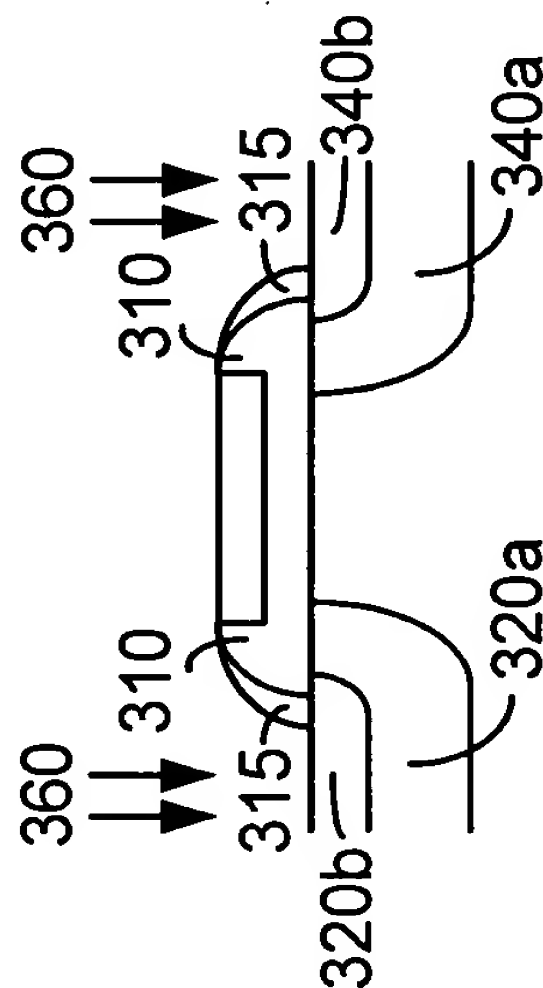
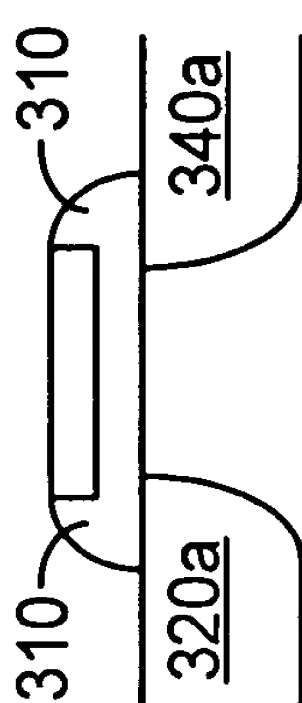
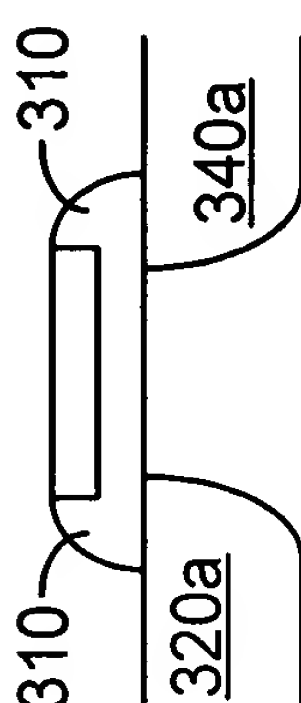
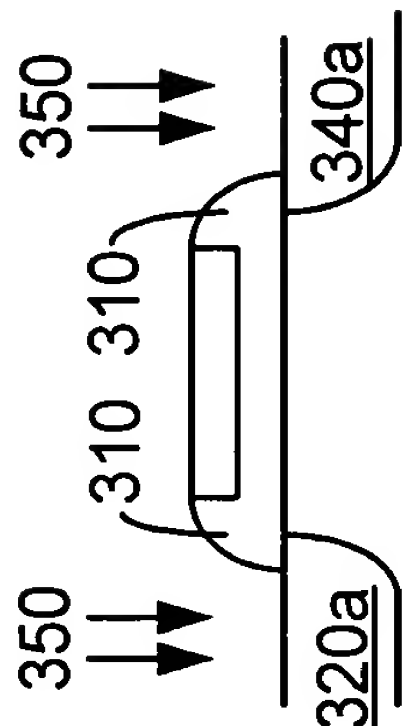
**Fig. 2d**



Periphery LDD  
LV transistor



Periphery DDD  
HV transistor



Array Cell

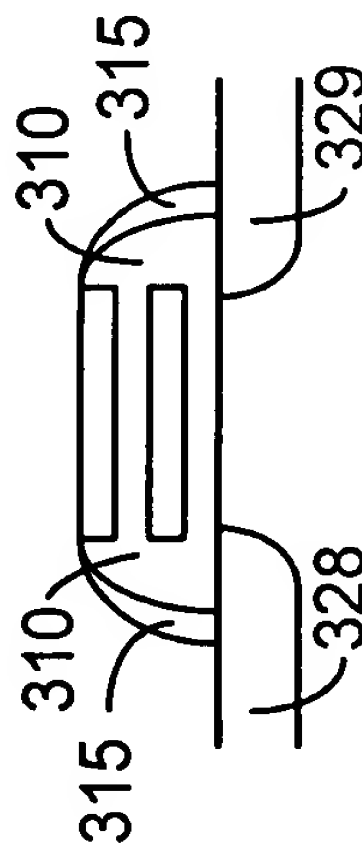
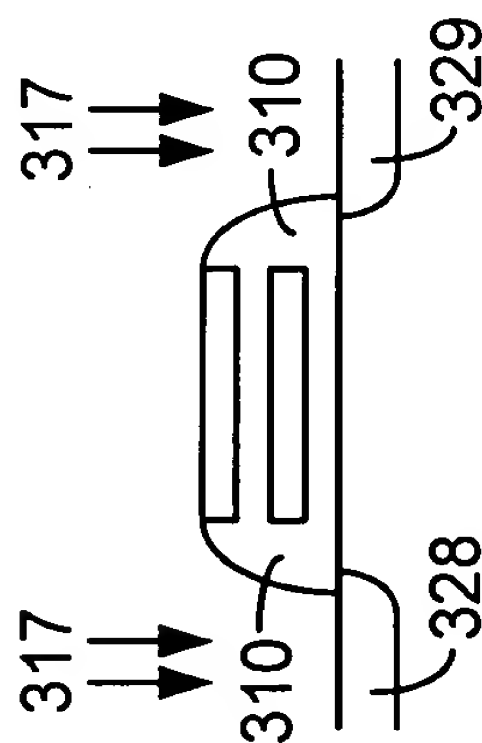
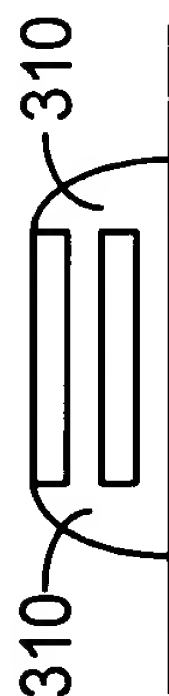
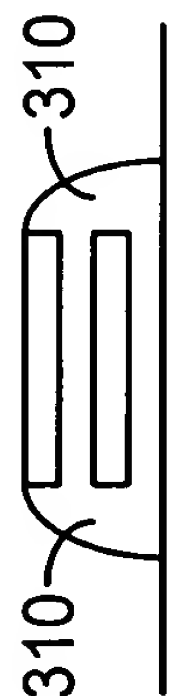


Fig. 3a

Fig. 3b

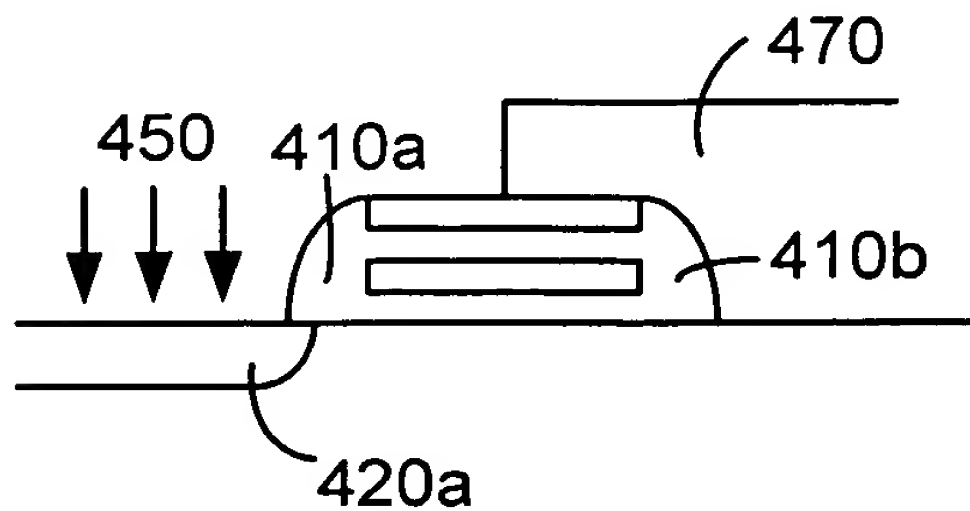
Fig. 3c

Fig. 3d

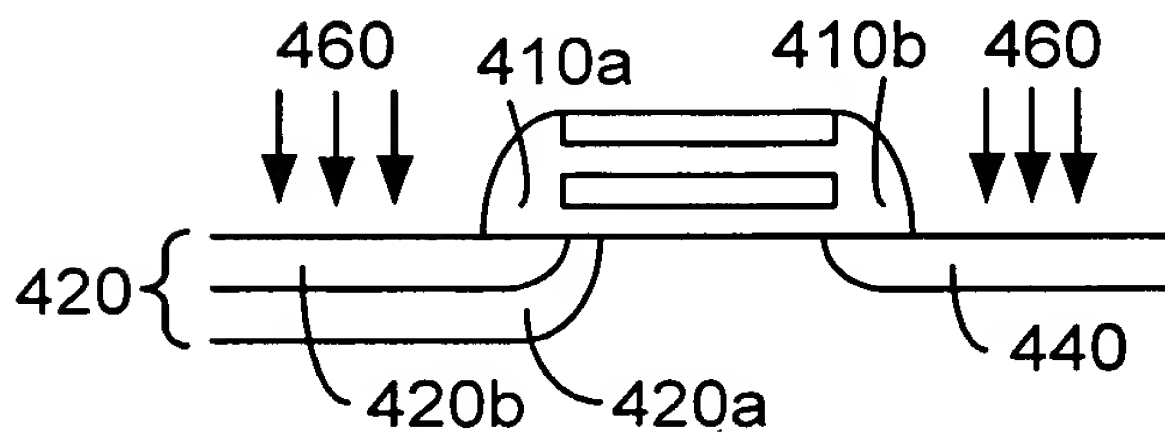


5/6

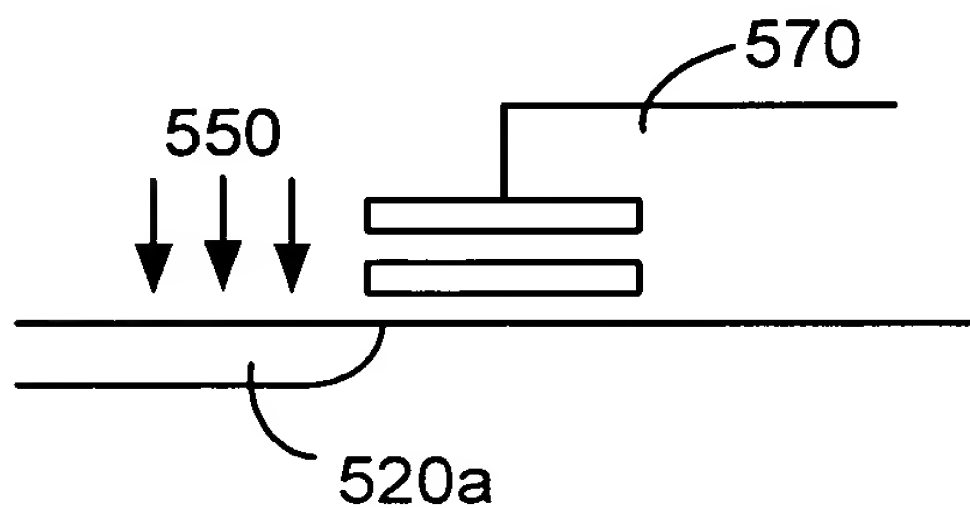
**Fig. 4a**



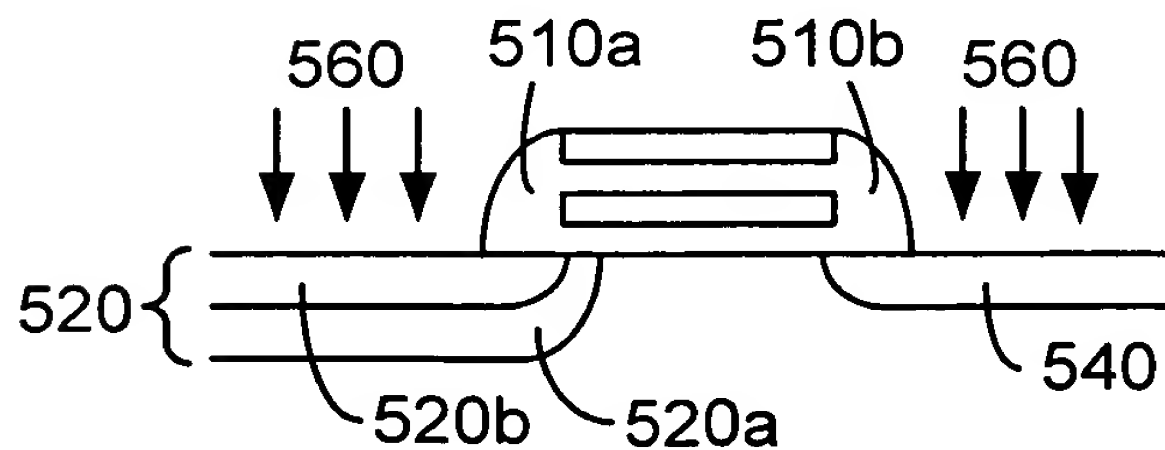
**Fig. 4b**

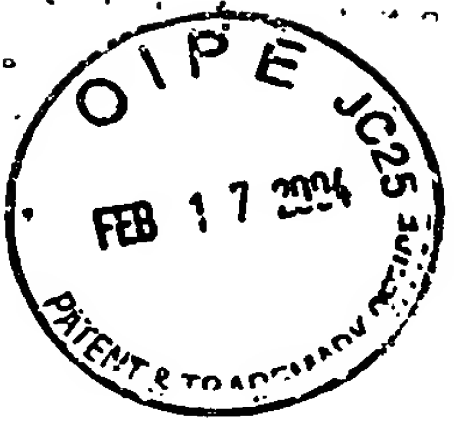


**Fig. 5a**

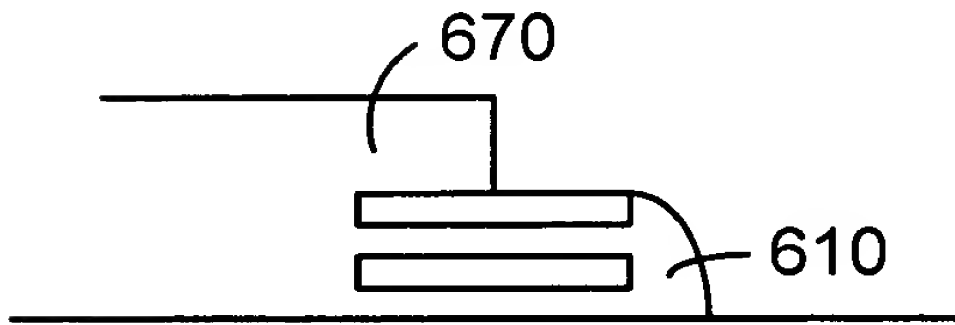


**Fig. 5b**





**Fig. 6**



**Fig. 7**

